IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	D.B. Kramer et al.
Case:	9-22
Serial No.:	10/085,222
Filing Date:	February 28, 2002
Group:	2616
Examiner:	Saba Tsegaye
Title:	Processor with Table-Based Scheduling Using Software-Controlled Interval Computation

---

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") hereby appeal the final rejection dated August 21, 2006 of claims 1-21 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on February 28, 2002 with claims 1-21. Claims 1-21 are currently pending in the application. Claims 1, 20 and 21 are the independent claims.

Each of claims 1-21 stands rejected under 35 U.S.C. §103(a). Claims 1-21 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising scheduling circuitry, including a hardware-implemented scheduler, and a software-implemented interval computation element external to the hardware-implemented scheduler. The scheduling circuitry schedules data blocks for transmission from a plurality of transmission elements and is configurable for utilization of at least one time slot table in scheduling the data blocks for transmission. The interval computation element determines an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table. A particular location in the time slot table is assigned to one or more of the transmission elements as a function of both a current time and the transmission interval and the transmission interval may be adjusted by the interval computation element so as to facilitate maintenance of a desired service level for one or more of the transmission elements. This adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone. With reference to FIG. 5 of the drawings, the recited processor may be network processor 102, the recited scheduling circuitry and interval computation element may be elements 306 and 504, respectively, and the time slot table may be element 506. See the specification at, for example, page 10, line 8, to page 12, line 3.

Independent claim 20 is directed to a method for use in a processor comprising a step of scheduling data blocks for transmission from a plurality of transmission elements wherein the scheduling step utilizes at least one time slot table to schedule the data blocks for transmission in

accordance with a determined interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval, the transmission interval being adjustable so as to facilitate maintenance of a desired service level for one or more of the transmission elements. The claim also recites that the scheduling step is performed in a hardware-implemented scheduler, the transmission interval is determined in a software-implemented interval computation element external to the hardware-implemented scheduler, and adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone. An illustrative embodiment of the recited arrangement can be found in FIG. 6 of the drawings, wherein the scheduling step is represented by blocks 602 through 612. See the specification at, for example, page 12, line 8, to page 13, line 9.

Independent claim 21 is directed to an article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements utilizing at least one time slot table, the one or more programs when executed providing at least one of determination of an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval, and adjustment of the interval so as to facilitate maintenance of a desired service level for one or more of the transmission elements. The claim also recites that the scheduling step is performed in a hardware-implemented scheduler, the transmission interval is determined in a software-implemented interval computation element external to the hardware-implemented scheduler, and adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone. With reference to FIG. 1 of the drawings, the processor in an illustrative embodiment may be network processor 102 and the machine-readable storage medium may comprise, for

example, internal memory 104, external memory 106, or combinations thereof. See the specification at, for example, page 4, line 28, to page 5, line 3, page 8, lines 4-6, and page 9, line 23, to page 10, line 2.

The claimed invention provides a number of significant advantages over conventional arrangements. For example, the recited arrangement of a hardware-implemented scheduler and a software-implemented interval computation element advantageously permits particularly efficient implementation of a variety of different scheduling algorithms. See the specification at, for example, page 3, lines 15-21, and page 12, line 11, to page 13, line 3.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 2, 4-18, 20 and 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,389,019 (hereinafter "Fan") in view of U.S. Patent No. 6,374,405 (hereinafter "Willard.")

2. Claims 1, 4, 14, 19 and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,889,763 (hereinafter "Boland") in view of Willard.

3. Claim 3 stands rejected under 35 U.S.C. §103(a) over Fan in view of Willard and further view of U.S. Patent No. 5,455,948 (hereinafter "Poole.")

4. Claim 19 stands rejected under 35 U.S.C. §103(a) over Fan in view of Willard and in further view of Boland.

ARGUMENT

1. §103(a) Rejection of Claims 1, 2, 4-18, 20 and 21 over Fan and Willard

Claims 1, 2, 4-7, 9-18, 20 and 21

A proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See MPEP § 706.02(j).

Appellants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in that Fan, when combined with Willard, fails to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or for modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

The Examiner concedes that Fan fails to disclose the limitations found in claim 1 of a software-implemented interval computation element external to a hardware-implemented scheduler wherein adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler. Instead, on page 3 of the final Office Action, Examiner contends that these limitations are disclosed by Willard. More specifically, the Examiner relies on the teachings in column 6, line 50, to column 7, line 12 of Willard which provide in part as follows:

> In one embodiment, the scheduler is implemented in software. The software executes on a microprocessor or microcontroller in the broadcast station. In other embodiments, the scheduler may be implemented in software, firmware, hardware or a combination thereof. The software implementation is readily adaptable to alternate embodiments in which the delivery time and transmission interval are not explicitly provided to the scheduler. In these embodiments, the interval and start time may be calculated from information such as module size, transmission bit rate and number of modules being simultaneously transmitted. For example, the interval may be calculated by dividing the size of the module by the transmission bit rate and then multiplying it by the number of modules being transmitted at the same time.

It is respectfully submitted that the portion of Willard quoted above fails to teach or suggest the software-implemented interval computation element external to a hardware-implemented scheduler as set forth in claim 1. It does teach that a scheduler can be implemented

in hardware, but fails to teach or suggest that a hardware-implemented scheduler can be advantageously combined with a software-implemented interval computation element external to the hardware-implemented scheduler, so as to implement time slot table based scheduling algorithms not otherwise supported by the hardware-implemented scheduler. To the contrary, the above portion of Willard appears to teach away from the claim limitation at issue by teaching, for example, a software-implemented scheduler that itself computes a transmission interval.

The Examiner places great weight on Willard's passing mention that "[i]n other embodiments, the scheduler may be implemented in software, firmware, hardware or a combination thereof." Appellants submit that this statement fails to suggest the modifications to the prior art that would be necessary to reach this invention. More particularly, this statement fails to provide any suggestion that the particular combination claimed in the instant application, namely the use of a software-implemented interval computation element in conjunction with a hardware-implemented scheduler based on time slot tables, is any more desirable than any other combination of software, firmware and hardware. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. See, e.g., In re Mills, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990) (Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so."). See also In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992).

Appellants submit that the present scenario is analogous to one which arises frequently in the chemical context, wherein the fact that a claimed species or subgenus is encompassed by a prior art genus is not sufficient by itself to establish a *prima facie* case of obviousness. See, e.g., In re Baird, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994) ("The fact that a claimed compound may be encompassed by a disclosed generic formula does not by itself render that compound obvious.").

Appellants alone have determined that such an arrangement provides significant advantages over conventional time slot table based scheduler implementations. For example, software control of the interval for transmission of data blocks associated with particular

locations in a time slot table can allow the hardware-implemented scheduler to support multiple scheduling algorithms not otherwise supported by the hardware-based scheduler alone. See the specification at, for example, page 11, line 21, to page 12, line 3, and page 12, lines 11-18. The proposed combination of Fan with Willard does not meet this particular limitation of claim 1, and fail to provide the associated advantages.

Appellants also note that Fan fails to teach or suggest the limitation of claim 1 relating to a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval. The Examiner relies on column 8, line 61, to column 9, line 6, and column 9, lines 10-21 of Fan. Appellants respectfully submit that this relied-upon portion of Fan fails to disclose assigning a location in the time slot table to one or more transmission elements, much less said location being assigned as a function of both a current time and a transmission interval. To the contrary, the scheduling mechanism disclosed in Fan simply maintains ready lists of eligible stream queues. See Fan at column 8, lines 54-56 and column 9, lines 16-24.

It is thus believed that the collective teachings of Fan and Willard fail to meet the limitations of claim 1 and fail to provide the associated advantages in terms of enhanced scheduling algorithm flexibility for a given hardware-implemented scheduler.

With regard to motivation to combine Fan with Willard, the Examiner provides the following statement in the final Office Action on pages 3 and 7-8:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings from Willard of using the combination of software-implemented element and hardware-implemented scheduler to the time-base scheduler discloses [sic] by Fan. One of ordinary skill in the art would have been motivated to do this because using the combination of software and hardware system [sic] provides a flexible and scalable architecture, improves performance and provides extended lifespan of the device.

Appellants respectfully submit that the proffered statement fails to provide sufficient objective motivation for the combination. The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an Examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. The statement listed above is believed to be a conclusory statement based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the statement above is using the benefit obtained from a combination as a motivation for that combination, and is therefore based on impermissible hindsight. See, e.g., In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (holding that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.)

As indicated previously, the particular separation of time slot table based scheduling circuitry into hardware-implemented scheduler and software-implemented interval computation element, and its attendant advantages, are not met by the proposed combinations. The general statements in Willard regarding possible implementation of a scheduler in "software, firmware, hardware or a combination thereof" fail to motivate modification of Fan to meet the particular limitations of claim 1 regarding advantageous implementation of a scheduler and an associated external interval computation element.

Additionally, Appellants respectfully submit that Willard is not analogous prior art in that is does not relate to time slot table based scheduling. See, e.g., MPEP § 2141.01(a); In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992) ("In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned."); In re Clay, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a

different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem."). The mere presence of the word "scheduling" in the title of both the instant application and Willard is insufficient to establish that they are analogous art; see, e.g., Wang Lab. v. Toshiba Corp., 993 F.2d 858, 864 (Fed. Cir. 1993) (holding that "art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories."). Willard has nothing to do with time slot table based scheduling, and those skilled in the art would therefore not have been motivated to look to Willard for teachings on how to implement time slot table based scheduling circuitry.

Independent claims 20 and 21 are believed allowable for reasons similar to those outlined above with regard to claim 1.

With regard to dependent claims 2, 4-7 and 9-18, which depend from claim 1, Appellants assert that these claims are also patentable over the prior art of record by virtue of their dependency from claim 1.

Claim 8

Dependent claim 8 recites an additional limitation wherein the interval computation element is operative to select the transmission interval from at least a first transmission interval associated with a first scheduling algorithm and a second transmission interval associated with a second scheduling algorithm. In formulating this rejection, the Examiner relies primarily on the teachings in column 9, line 54, to column 10, line 21, of Fan. However, the relied upon portion of Fan fails to meet the particular limitations at issue, in that it fails to teach or suggest the use of multiple scheduling algorithms to compute multiple transmission intervals, one of which may then be selected.

Instead, the cited portions of Fan teach the use of a coarse-grained time wheel and a fine grained time wheel to reduce the amount of memory needed to store the time wheels in order to support a range of transmission rates. They do not suggest the calculation of first and second transmission intervals using respective first and second scheduling algorithms as recited. See

Fan at column 9, lines 25-45. Accordingly, it is believed that the collective teachings of Fan and Willard fail to render claim 8 obvious as alleged.

2. §103(a) Rejection of Claims 1, 4, 14, 19 and 20 over Boland and Willard

Appellants submit that the Examiner has again failed to establish a proper *prima facie* case of obviousness, in that Boland, if combined with Willard, fails to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or for modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

The Examiner concedes that Boland fails to disclose the limitations found in claim 1 of a software-implemented interval computation element external to a hardware-implemented scheduler wherein adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler. Instead, on page 7 of the final Office Action, Examiner contends that these limitations are disclosed by Willard. More specifically, the Examiner relies on the teachings in column 6, line 50, to column 7, line 12 of Willard which provide in part as follows:

> In one embodiment, the scheduler is implemented in software. The software executes on a microprocessor or microcontroller in the broadcast station. In other embodiments, the scheduler may be implemented in software, firmware, hardware or a combination thereof. The software implementation is readily adaptable to alternate embodiments in which the delivery time and transmission interval are not explicitly provided to the scheduler. In these embodiments, the interval and start time may be calculated from information such as module size, transmission bit rate and number of modules being simultaneously transmitted. For example, the interval may be calculated

by dividing the size of the module by the transmission bit rate and then multiplying it by the number of modules being transmitted at the same time.

It is respectfully submitted that the portion of Willard quoted above fails to teach or suggest the software-implemented interval computation element external to a hardware-implemented scheduler as set forth in claim 1. It does teach that a scheduler can be implemented in hardware, but fails to teach or suggest that a hardware-implemented scheduler can be advantageously combined with a software-implemented interval computation element external to the hardware-implemented scheduler, so as to implement time slot table based scheduling algorithms not otherwise supported by the hardware-implemented scheduler. To the contrary, the above portion of Willard appears to teach away from the claim limitation at issue by teaching, for example, a software-implemented scheduler that itself computes a transmission interval.

The Examiner places great weight on Willard's passing mention that "[i]n other embodiments, the scheduler may be implemented in software, firmware, hardware or a combination thereof." Appellants submit that this statement fails to suggest the modifications to the prior art that would be necessary to reach this invention. More specifically, this statement fails to provide any suggestion that the combination claimed in the instant application, namely the use of a software-implemented interval computation element in conjunction with a hardware-implemented scheduler based on time slot tables, is any more desirable than any other combination of software, firmware, and hardware. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. See, e.g., In re Mills, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990) (Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so."). See also In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992).

Appellants submit that the present scenario is similar to one which arises frequently in the chemical context, wherein the fact that a claimed species or subgenus is encompassed by a prior art genus is not sufficient by itself to establish a *prima facie* case of obviousness. See, e.g., In re

Baird, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994) ("The fact that a claimed compound may be encompassed by a disclosed generic formula does not by itself render that compound obvious.").

Appellants alone have determined that such an arrangement provides significant advantages over conventional time slot table based scheduler implementations. For example, software control of the interval for transmission of data blocks associated with particular locations in a time slot table can allow the hardware-implemented scheduler to support multiple scheduling algorithms not otherwise supported by the hardware-based scheduler alone. See the specification at, for example, page 11, line 21, to page 12, line 3, and page 12, lines 11-18. The proposed combination of Boland with Willard does not meet this particular limitation of claim 1, and fails to provide the associated advantages.

Appellants note that page 7 of the final Office Action fails to identify any particular portion of Boland which is alleged to teach or suggest the limitation of claim 1 relating to a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval. There is no teaching or suggestion in Boland regarding this particular limitation. To the contrary, the timetables 100 and 200 in Boland comprise entries which associate "some number of time slots with lists of transfer context designators or virtual connection designators." See Boland at column 2, lines 51-59. It is thus believed that the collective teachings of Boland and Willard fail to meet the limitations of claim 1 and fail to provide the associated advantages in terms of enhanced scheduling algorithm flexibility for a given hardware-implemented scheduler.

With regard to motivation to combine Boland with Willard, the Examiner provides the following statement in the final Office Action on pages 7-8:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings from Willard of using the combination of software-implemented element and hardware-implemented scheduler to the time-base scheduler discloses [sic] by Boland. One of ordinary skill in the art would have been motivated to do this because using the

> combination of software and hardware system [sic] provides a flexible and scalable architecture, improves performance and provides extended lifespan of the device.

Appellants respectfully submit that the proffered statement fails to provide sufficient objective motivation for the combination. The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an Examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. The statement listed above is believed to be a conclusory statement based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the statement above is using the benefit obtained from a combination as a motivation for that combination, and is therefore based on impermissible hindsight. See, e.g., In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (holding that the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.)

As indicated previously, the particular separation of time slot table based scheduling circuitry into hardware-implemented scheduler and software-implemented interval computation element, and its attendant advantages, are not met by the proposed combinations. The general statements in Willard regarding possible implementation of a scheduler in "software, firmware, hardware or a combination thereof" fail to motivate modification of Boland to meet the particular limitations of claim 1 regarding advantageous implementation of a scheduler and an associated external interval computation element.

Additionally, Appellants respectfully submit that Willard is not analogous prior art in that is does not relate to time slot table based scheduling. See, e.g., MPEP § 2141.01(a); In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992) ("In order to rely on a

reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned."); In re Clay, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem."). The mere presence of the word "scheduling" in the title of both the instant application and Willard is insufficient to establish that they are analogous art; see, e.g., Wang Lab. v. Toshiba Corp., 993 F.2d 858, 864 (Fed. Cir. 1993) (holding that "art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories."). Willard has nothing to do with time slot table based scheduling, and those skilled in the art would therefore not have been motivated to look to Willard for teachings on how to implement time slot table based scheduling circuitry.

Independent claim 20 is believed allowable for reasons similar to those outlined above with regard to claim 1.

Dependent claims 4, 14 and 19 are believed allowable at least by virtue of their dependency from claim 1.

3. §103(a) Rejection of Claim 3 over Fan, Willard and Poole

Dependent claim 3 further specifies that the interval computation element of claim 1 comprises a script processor. The Examiner concedes that neither Fan nor Willard teach this additional claim limitation; instead, the Examiner contends that "Pool [sic] teaches a processor wherein priority computation element comprises of [sic] a script processor." Appellants respectfully suggest that the priority computation element of Poole is not suggestive of the interval computation element of the present invention. Rather, Poole discloses the use of a script processor to "provide a way for the user interface component of an application program to operate independent of data and the source of the data." (Poole, column 3, lines 24-28). Both the client and server have their own script processor whose job is to act as an interface layer between an application and its data source (Poole, column 7, lines 10-16 and FIG. 3). The queuing and

scheduling facility of the script processor as disclosed in Poole refers not to queuing and scheduling data for transmission over a network between client and server, but rather to queuing and scheduling of jobs (applications) on the server. There is thus no motivation to combine the teachings and the combined teachings still fail to suggest each and every element of the claim.

Additionally, Appellants respectfully submit that Poole is not analogous prior art in that is does not relate to time slot table based scheduling. See, e.g., MPEP § 2141.01(a); In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992) ("In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned."); In re Clay, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem."). Poole has nothing to do with time slot table based scheduling, and those skilled in the art would therefore not have been motivated to look to Poole for teachings on how to implement time slot table based scheduling circuitry.

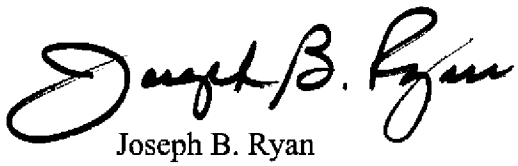
Additionally, Appellants assert that claim 3 is patentable over the prior art of record by virtue of dependency from its base claim 1, which is believed to be patentable for at least the reasons given above.

4. §103(a) Rejection of Claim 19 over Fan, Willard and Boland

Appellants assert that claim 19 is patentable over the prior art of record by virtue of its dependency from its base claim 1, which is believed to be patentable for at least the reasons given above. Furthermore, Appellants respectfully submit that the instant rejection over the combined teachings of Fan, Boland and Willard suffers from the same defects identified above with regard to the separate combinations of Fan with Willard and Boland with Willard.

In view of the above, Appellants believe that claims 1-21 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejections.

Respectfully submitted,



Date: January 22, 2007

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

CLAIMS APPENDIX

1. A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements, the scheduling circuitry being configurable for utilization of at least one time slot table in scheduling the data blocks for transmission; and

an interval computation element associated with the scheduling circuitry and operative to determine an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval, the transmission interval being adjustable under control of the interval computation element so as to facilitate maintenance of a desired service level for one or more of the transmission elements;

wherein the scheduling circuitry comprises a hardware-implemented scheduler;

wherein the interval computation element comprises a software-implemented element external to the hardware-implemented scheduler; and

wherein adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone.

2. The processor of claim 1 wherein the interval computation element operates under software control in at least one of determining and adjusting the transmission interval.

3. The processor of claim 1 wherein the interval computation element comprises a script processor.

4. The processor of claim 1 wherein the interval computation element is operative to determine periodically if the transmission interval requires adjustment in order to maintain the desired service level for one or more of the transmission elements.

5. The processor of claim 4 wherein the interval computation element makes a determination as to whether the transmission interval requires adjustment, after transmission of a specified number of the data blocks.

6. The processor of claim 5 wherein the interval computation element makes the determination as to whether the transmission interval requires adjustment after transmission of each of the data blocks.

7. The processor of claim 1 wherein the transmission interval specifies a rate at which data blocks associated with corresponding locations in the time slot table are transmitted.

8. The processor of claim 1 wherein the interval computation element is operative to select the transmission interval from at least a first transmission interval associated with a first scheduling algorithm and a second transmission interval associated with a second scheduling algorithm.

9. The processor of claim 1 wherein a given requesting transmission element is assigned to a location in the time slot table in accordance with the following equation:

$$\text{Assigned Time Slot} = \text{Current Time} + \text{Interval},$$

where Current Time denotes a time corresponding to a current transmission time slot and Interval denotes the transmission interval.

10. The processor of claim 1 wherein the scheduling circuitry comprises the time slot table.

11. The processor of claim 1 further comprising traffic shaping circuitry coupled to the scheduling circuitry, the traffic shaping circuitry comprising the interval computation element.

12. The processor of claim 11 further comprising transmit queue circuitry coupled to the scheduling circuitry, wherein the transmission elements comprise one or more queues associated with the transmit queue circuitry, the transmit queue circuitry supplying time slot requests from the transmission elements to the scheduling circuitry in accordance with a traffic shaping requirement established by the traffic shaping circuitry.

13. The processor of claim 1 wherein the time slot table is stored at least in part in an internal memory of the processor.

14. The processor of claim 1 wherein the time slot table is stored at least in part in an external memory coupled to the processor.

15. The processor of claim 1 wherein one or more of the data blocks comprise data packets.

16. The processor of claim 1 wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand basis.

17. The processor of claim 16 wherein the identifiers of the transmission elements comprise a structure having one or more bits for allowing a given one of the transmission element identifiers to be linked to another of the transmission element identifiers.

18. The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

19. The processor of claim 1 wherein the processor is configured as an integrated circuit.

20. A method for use in a processor, the method comprising:

scheduling data blocks for transmission from a plurality of transmission elements;

wherein the scheduling step utilizes at least one time slot table to schedule the data blocks for transmission in accordance with a determined interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, a particular location in the time slot table being assigned to one or more of the transmission elements as a function of both a current time and the transmission interval, the transmission interval being adjustable so as to facilitate maintenance of a desired service level for one or more of the transmission elements;

wherein the scheduling step is performed in a hardware-implemented scheduler;

wherein the transmission interval is determined in a software-implemented interval computation element external to the hardware-implemented scheduler; and

wherein adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone.

21. An article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements utilizing at least one time slot table, the one or more programs when executed providing at least one of determination of an interval for transmission of one or more data blocks associated with corresponding locations in the time slot table, a particular location in the time slot table being

assigned to one or more of the transmission elements as a function of both a current time and the transmission interval, and adjustment of the interval so as to facilitate maintenance of a desired service level for one or more of the transmission elements;

wherein the scheduling is performed in a hardware-implemented scheduler;

wherein the transmission interval is determined in a software-implemented interval computation element external to the hardware-implemented scheduler; and

wherein adjustment of the transmission interval by the interval computation element allows the hardware-implemented scheduler to support at least one scheduling algorithm not otherwise supported by the hardware-implemented scheduler alone.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None